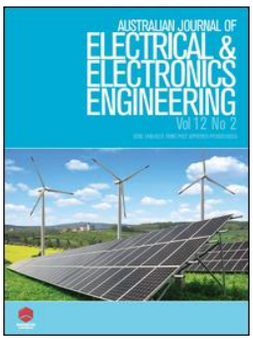

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ARTICLE

A survey of leakage reduction techniques in CMOS digital circuits for nanoscale regime

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ABSTRACT

The battery-driven portable systems are the lifeline of the modern era. Very large-scale integration (VLSI) designers are continuously working to enhance the performance of the portable systems. The small size, fast response and high battery back-up are the prime factors for the portable systems. Scaling down of the metal oxide semiconductor field effect transistor (MOSFET) dimensions is mandatory to design the low size systems. The power supply and the threshold voltage must be scaled-down with each new technology node in order to maintain the performance of the devices. The scaling down of the threshold voltage of the device produces leakage current. The amount of the leakage current is large at integration level and harms the characteristics of the systems. Therefore, leakage current mitigation is needed especially at lower technology nodes to boost the battery back-up of the portable systems. Number of leakage reduction techniques are available at different abstraction levels. In this review paper, a systematic flow of the low power VLSI field is explored with the target of the different existing circuit level leakage reduction techniques. NAND3 gate is designed and simulated at 16 nm technology node by using the different existing leakage reduction techniques for the comparison purpose.

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KEYWORDS
Low power VLSI; nanoscale regime; leakage power; CMOS; circuit level technique

1. Introduction

High-performance, low leakage integrated circuits (ICs) are the backbone of the electronic industry. Number of electronic devices are fabricated on a semiconductor wafer to form an IC. IC increases the functionality of the systems on a small wafer area (Sharma and Pattanaik 2016). Therefore, small size and fast response conditions for the electronic systems are achieved with the help of ICs. The area efficient IC needs the shrinking of the MOSFET size by a scaling factor so that large number of the devices can be integrated on a small area (Ferain, Colinge, and Colinge 2011; Ratnesh et al. 2021). The integration of the devices follows Moore's prediction where device density on an IC doubles after every two years without any cost penalty (Moore 1998).

The integration of the semiconductor devices on a small silicon wafer is possible only when the dimensions of the electronic devices are scaled-down. The power supply and the threshold voltage of the devices must be scaled-down for the lower technology nodes. Leakage current is inversely proportional to the threshold voltage. Scaling-down of the threshold voltage for the lower technology nodes produces large leakage current (Sharma and Pattanaik 2014; Gundu and Kursun 2021). Hence, the power dissipation of the devices is rising at lower technology nodes. 40% of the power consumption is dissipated as the leakage power for the processor designed at 65 nm (Bhunia and Mukhopadhyay 2011).

In nanoscale regime, leakage current is a challenging issue for the low power VLSI designers (Ahmad et al. 2017). Large leakage current changes the characteristics of the electronic systems and disturbs the reliability, the managing cost of the ICs (Shauly 2012; Mahmoud and Soin 2019). Hence, leakage current reduction is mandatorily needed in nanoscale regime. Low power VLSI is a key research area for the current electronic industry to explore the possible solutions for the large leakage current mitigation. The design of the low power VLSI circuits enhances the overall performance of the battery-driven portable systems such as laptop, mobile phone, portable medical equipment, calculator etc.

Complementary metal oxide semiconductor (CMOS) logic is commonly employed for the ICs because of numerous advantages as compared to other logics. The few key benefits of the CMOS logic are high noise immunity, low leakage power, easy fabrication, high device density, low complexity, full rail to rail output etc. CMOS logic comprises two power dissipation components: dynamic and static power dissipation. The current flows during the logic transitions is identified as dynamic current which originates dynamic power dissipation. Static current flows during the static logic levels and accumulates the static power dissipation. Dynamic power dissipation is the major part of the total power

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dissipation when technology nodes are generally above 100 nm. But, present electronic industry is working for the below 100 nm technology nodes. Therefore, static or leakage power dissipation is the key part of the total power dissipation in below 100 nm technology nodes.

Low power VLSI designers are investigating the different options to minimise the leakage current in nanoscale regime because leakage current harms the reliability of the systems if it exceeds the expected level. The operation of the IC may be damaged if the amount of the leakage current is large. Large leakage current raises the heating issue which may damage the system's functions. So, leakage mitigation technique avoids the heating issue of the systems (Sharma and Pattanaik 2013). Low power VLSI design is the most demanded area for today's scenario to find the low leakage options. Many researchers are applying their innovative ideas for leakage reduction in nanoscale regime (Kumar and Tripathi 2021).

This review paper presents an extensive knowledge of the field of low power VLSI design. The need of the field, background of the field, development in the field and the future prospect of the field are comprehensively discussed. The comprehensive study of the existing leakage mitigation techniques at circuit level is provided. The general ideas of the different leakage reduction techniques are applied to simulate a NAND3 gate at 16 nm technology node for the comparison purpose.

The rest of the paper is organised as: the device scaling methods are explained in section 2. The various important leakage current components are given in section 3. Section 4 discusses the operation of the different leakage mitigation techniques. The comparative analysis among the techniques is presented in section 5. Finally, the paper is concluded in section 6.

2. Scaling methods for MOSFET

MOSFET scaling is the significant process to design the high-density ICs. G. E. Moore has predicted the nature of device density on the semiconductor wafer.The idea for the MOSFET scaling was proposed by Robert Dennard (Dennard et al. 1999; Ning 2007). The electronic industry achieves a lot because of the device scaling. The device scaling makes possible to generate the large number of functions on a small semiconductor wafer (Bohr and Young 2017). A MOSFET device has number of scalable parameters. Hence, all the horizontal and vertical dimensions of the MOSFET device are systematically scaled by a constant parameter. This constant parameter is termed as scaling factor and commonly represented as S. S must be greater than 1.

MOSFET scaling is not only increasing the device density on an IC but also decreases the propagation delay of the transistor. The scaling of the different device parameters causes to reduce the barrier potential between the drain and the source terminals. It reduces the threshold voltage and hence the scaled MOSFET operates fast. So, device speed is improved for each new technology node generation (Kajal and Sharma 2021). The broad categories of the scaling methods are constant field and constant voltage scaling. These scaling methods are categorised on the basis of specific constant parameter value. The device characteristic behaves differently for the different scaling methods. Both types of the scaling methods have their merits and demerits. Both the scaling methods are briefly explained as:

2.1. Constant field

The internal electric field is the constant parameter in case of constant field scaling method.Hence, all the device dimensions are scaled by the factor S while forwarding the same internal electric field for the scaled devices. It is the widely used scaling method as compared to constant voltage because of numerous advantages such as unchanged power density, less power dissipation, less heating issue, low parasitic capacitances and performance improvement. Sometimes, constant field scaling is also called as full scaling (Stork 2007). Full scaling scales all the voltage levels of the device. It means threshold voltage is also scaled by the factor S. But, reduction in threshold voltage causes large sub-threshold leakage current (Frank et al. 2001). The full scaling of the important device parameters is presented in Table 1.

2.2. Constant voltage

All the voltage levels associated with the device are scaled by a factor S in full scaling method. Sometimes, it limits the operation of the complicated voltage levels specially in interface circuits. This is the limitation of the full scaling method. Constant voltage scaling overcomes this limitation by keeping the same voltage level for the scaled devices. In constant voltage scaling method, all the horizontal and vertical dimensions of the device are scaled by S while maintaining the constant value of the voltage levels. Table 1 shows the constant voltage scaling of the different important parameters.Few disadvantages of the constant voltage

Table 1. Scaled key device parameters.

Device parameter	Full scaling	Constant voltage scaling
Channel width	1/ S	1/ S
Channel length	1/ S	1/ S
Voltage level	1/ S	1
Threshold voltage	1/ S	1
Electric field	1	S
Doping for n-type and p-type	S	S^2
Gate oxide thickness	1/ S	1/ S
Oxide capacitance	S	S
Current	1/ S	S
Power dissipation	1/ S^2	S
Propagation delay	1/ S	1/ S^2
Power delay product	1/ S^3	1/ S
Power density	1	S^3

scaling method are high power density generation, which produces electro-migration, oxide breakdown, large power dissipation and hot-carrier degradation. The voltage level must be scaled for each new technology node to maintain the performance of the circuits. So, constant voltage scaling is rarely used below 800 nm technology nodes (Kursun and Friedman 2006).

The channel width, length, gate oxide thickness and oxide capacitance of the MOSFET device are scaled by the same scaling factor in both types of scaling methods. The charge-electric field equation is observed for the doping profiles and hence these are increasing in both scaling methods.Power delay product (PDP) is treated as figure of merit for the logic circuits. PDP has the least value in case of full scaling method. Hence, full scaling method is well balancing the trade-off between the power dissipation and speed which improves the overall characteristics of the logic circuits in nanoscale regime.

3. Parts of leakage current

The target of this review paper is to explore the different power saving methodologies in nanoscale regime. As static or leakage power dissipation is the dominant part of the total power dissipation in nanoscale regime so different leakage power saving schemes are discussed in this review paper.The Total power dissipation is the sum of the dynamic and static parts. Dynamic power dissipation associates switching and short-circuit power because both are related to the transition duration (Brzozowski and Kos 2008). The total power dissipation of the circuits is calculated as mentioned in equation 1.

$$P_{DISSIPATION} = P_{SWITCHING} + P_{SHORTCIRCUIT} + P_{LEAKAGE} \quad (1)$$

The charging and discharging of the load capacitance of the CMOS logic circuit produces switching power dissipation ($P_{SWITCHING}$). The charging and discharging of the load capacitance are depending on the primary inputs. If the primary inputs of the CMOS logic are in such a way that the pull-up network (PUN) and the pull-down network (PDN) of the CMOS logic conduct simultaneously then short-circuit power dissipation ($P_{SHORTCIRCUIT}$)is generated. The amount of $P_{SHORTCIRCUIT}$ is large for the large rise and fall times. $P_{LEAKAGE}$ is the product of power supply voltage and the leakage current. Leakage current is the addition of the number of leakage parts.

In nanoscale regime, MOSFET exhibits number of leakage parts. These leakage parts are depending on the different factors owing to geometrical structure and the operating environment. Figure 1 depicts the different leakage parts in NMOS device (Ekekwe and Etienne-Cummings 2006).

In Figure 1, $I_{REV}$is PNreverse bias current, $I_{GIDL}$is gate-induced drain leakage current, $I_P$is punch-through current, $I_{SUB}$is sub-threshold current, $I_G$is gate current and $I_H$is hot-carrier current.

The impact of these leakage parts is more in nanoscale regime. These leakage parts must be reduced for increasing the battery life of the portable electronic systems. I_{SUB}contributeshuge leakage current as compared to the others. Therefore, low power VLSI researchers are primarily focusing for the I_{SUB} reduction. The briefs of the different leakage parts are also provided in this review paper so that new researchers may understand the low power VLSI field in a fast pace.

3.1. 3.1PNReversebias current

The formation of the PN junctions between the diffused (N+) regions and the substrate (P) causes PN reverse bias current. It means I_{REV} depends on the areas of the diffused regions and minority charge carriers. Minority charge concentration gradient is mainly responsible for the tunnelling of the I_{REV}because it produces high electric field across the PN junction (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003).

3.2. GIDL current

In NMOS device, an accumulation of the holes in the channel region reduces the width of the depletion layer between the diffused region and the channel region.The application of the negative bias voltage at the gate terminal increases the accumulation of the holes in the channel region. If the power supply voltage is increased, then it further reduces the width of the depletion layer. For this type of the device setup, a leakage current path exists between the gate terminal and the substrate of the NMOS, which provides the path for the GIDL current. The main reason for this leakage part is minority charge carrier (Yuan et al. 2008). The mechanism of the GIDL is provided in Figure 2.

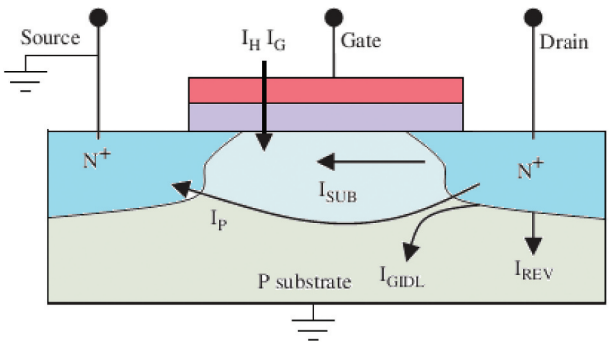

Figure 1. Leakage parts in NMOS device.

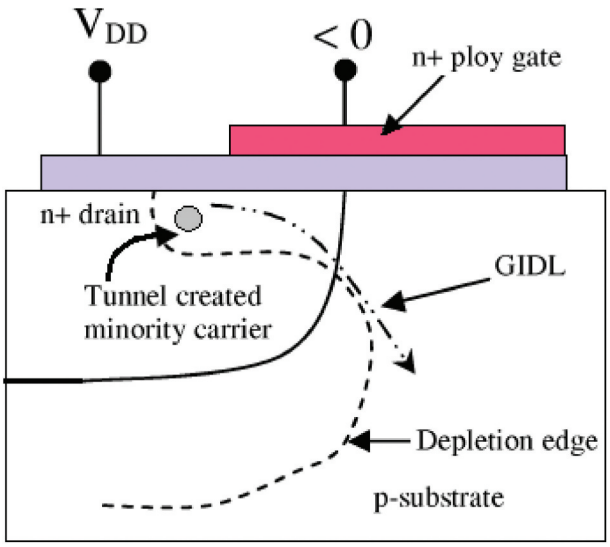

Figure 2. GIDL current path in NMOS device.

3.3. Punch-through current

Scaling is the chief process to enhance the performance of the devices for the advanced technology nodes. The scaling process scales the channel length with increased channel doping. It means the depletion layers of the source substrate and the drain substrate regions are possibly touching to each other. At this stage, I_P starts to flow (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003). $I_P$current is the function of the different MOSFET parameters which are presented in equation 2.

$$V_P \propto N_{SUB}\left(L - W_j\right)^3 \tag{2}$$

Where, V_P is the punch-through voltage, N_{SUB} is the substrate doping, L is the channel length and W_j is the junction width.

3.4. Sub-threshold current

Ideally, there is no current conduction when device is operating in off-state. Practically, small current conduction is present during the off-state of the devices. This current conduction is off-state current. For NMOS device, small current conduction is there even the gate voltage is less than the threshold voltage of the device. Therefore, this leakage part is also called as sub-threshold or weak inversion leakage current. This leakage part is the major part of the total leakage current and can't be ignored in nanoscale regime (Shauly 2012). Many researchers have been working to minimise this part as this is the key leakage part. The various device parameters can be used to mitigate this part. The expression for the sub-threshold current is given in equation 3.

$$I_{SUB} = \mu_0 C_{OX}\frac{w}{l}(m-1)V_T{}^2 e^{\frac{(V_{GS}-V_{TH})}{mV_T}}\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{3}$$

$$m = 1 + \frac{C_D}{C_{OX}} \tag{4}$$

$$V_T = \frac{kT}{q} \tag{5}$$

Where, μ_0 is the zero bias mobility, C_{OX} is the oxide capacitance, $\frac{w}{l}$ is the ratio of channel width to channel length, m is the sub-threshold swing factor, V_T is the thermal equivalent voltage, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, V_{DS} is the drain to source voltage and C_D is the depletion capacitance.

Another important parameter to boost the drive current for a givenoff-state current is sub-threshold slope. It finds the relation between the off-state current and the input voltage. Sub-threshold slope is the way which stops the flow of current if V_{GS} is less than V_{TH}. Least value of the sub-threshold slope is desirable (Vaddi, Dasgupta, and Agarwal 2010). It is measured in mV/decade. Figure 3 represents the sub-threshold slope for the NMOS device.

The expression for the sub-threshold slope is given in equation 6.

$$Sub - thresholdslope = 2.3\frac{KT}{q}\left(1 + \frac{C_D}{C_{OX}}\right) \tag{6}$$

Therefore, sub-threshold slope can be controlled by managing the different parameters as shown in Figure 6.

3.5. Gate current

Device scaling process impacts the characteristics preferably in the nanoscale regime. The scaling of the device dimensions in nanoscale regime reduces the oxide thickness. Hence, current conduction is possible

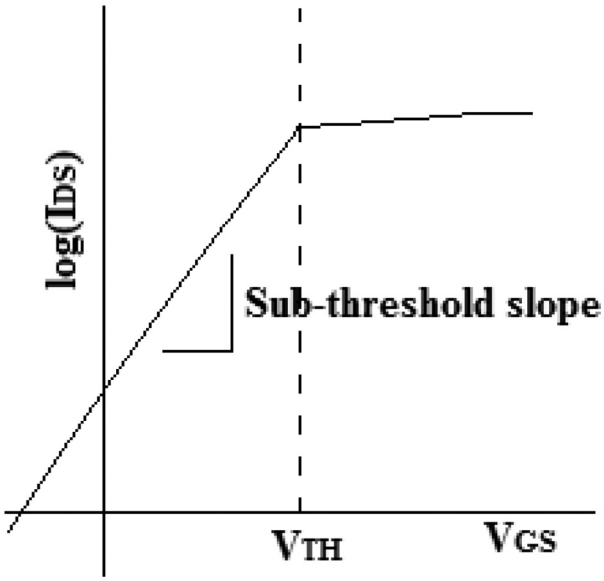

Figure 3. Sub-threshold slope for NMOS device.

between the gate and the substrate region and this current conduction is the gate leakage current (Lee, Blaauw, and Sylvester 2004; Elgharbawy and Bayoumi 2005). Gate current is the major part of the total leakage current after the sub-threshold current.The gate current expression is presented in equation 7 (Butzen et al. 2010).

$$I_G = wlA\left(\frac{V_{ox}}{t_{ox}}\right)^2 e^{\frac{(-B\left(1-\sqrt[3]{(1-(V_{ox}-\phi_{ox})}\right)}{V_{ox}/t_{ox}}} \quad (7)$$

$$A = (q)^3/16\pi^2 h\phi_{ox} \quad (8)$$

$$B = 4\pi\sqrt{2mox}\sqrt[3]{\phi_{ox}}/3hq \quad (9)$$

Where, q is the electron charge, h is the $1/2\pi$ X Planck's constant, ϕ_{ox} is the tunnelling barrier height, *mox* is the effective mass of the tunnelling particle, V_{ox} is the potential across the oxide and t_{ox} is the oxide thickness. Gate current can be minimised by the high-k dielectric material (Wong and Iwai 2006).

There are two reasons for the gate current tunnelling: direct and Fowler-Nordheim.The nature of the tunnelling is dependent on the energy-band diagram of the MOSFET.The difference between them is depicted in Figure 4.

V_{ox}isthepotentialacrosstheoxidelayerand$\phi_{ox}$is the tunnelling barrier height.The charge carriers flow through the trapezoidal shape in direct tunnelling while the charge carriers move through the triangular shape of the barrier potential inFowler-Nordheim tunnelling.

3.6. Hot-carrier current

Sometimes, hot-carrier current (I_H) is associated with the gate current because of the flowing nature. I_H flows between the oxide and the substrate regions due to high electric field across the oxide layer. High electric field provides the sufficient energy to the charge carriers to cross the barrier potential. The electric field is inversely proportional to the oxide thickness. The oxide thickness is scaled by a scaling factor in nanoscale regime and this process increases the electric field across the oxide. High electric field is solely responsible for the I_H current (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003). The electrons have the more mobility as compared to holes so, penetrates the oxide region more.

4. Leakage reduction techniques

The necessity of the low power VLSI design is increased more in the nanoscale regime. Leakage reduction techniques are the backbone of the low power VLSI design.The various researchers had worked for the different methodologies to mitigate the leakage current in nanoscale regime. The various abstraction levels are available in the low power VLSI design to deduct the different leakage parts. A circuit level method is the powerful methodology to reduce the leakage current at the cost of the increased number of transistors in a logic circuit. This review paper deals the key circuit level methods in low power VLSI design.The main device parameter is threshold voltage (V_{TH}) to deduct the leakage current at transistor or circuit level method (Butzen et al. 2010). V_{TH} is the function of the different parameters as shown in equation 10.

$$V_{TH} = V_{TH0} + K1\left[\sqrt{|2\phi_S| + V_{BS}} - \sqrt{|2\phi_S|}\right] - K2V_{BS} + \triangle \quad (10)$$

Where, V_{TH0} is the zero-body bias threshold voltage, K1 and K2 are the first and second order body bias coefficients, respectively, $2\phi_S$ is the surface potential, V_{BS} is the body to source voltage and $\triangle$ shows the small change in the device parameters.

The different key ideas for mitigating the leakage current at circuit level design are briefed in this section.There are broadly three concepts for the leakage

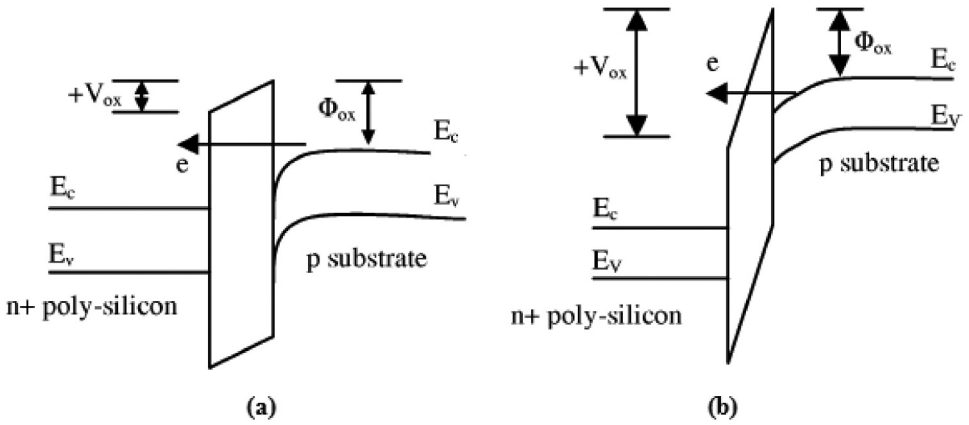

Figure 4. Gate leakage for NMOS (a) direct (b) Fowler-Nordheim tunneling.

reduction at circuit level design in low power VLSIfield. These broad concepts are transistors stack, multiple-threshold and body bias. These concepts are directly affecting the V_{TH} of the devices and hence, managing the leakage current. These broad concepts are the basis for the different leakage mitigation methods.

4.1. Transistors stack

Transistors stack is an efficient methodology to control the leakage current during the off-state of the transistors. In this methodology, number of transistors are connected in series configuration and operating in off-state. This type of the transistors arrangement increases the threshold voltage of the off-state transistors. Increment in the threshold voltage mitigates the off-state current and decreases the overall leakage current (Mukhopadhyay et al. 2003; Gu and Elmasry 1996). The logical path is not affected in the on-state of the devices due to the transistors stack.The transistors stack is formed by the extra insertion of the transistors. The extra insertion of the devices produces the issue of large propagation delay and lower drive current. Hence, sizing of the extra inserted devices pays a crucial role to manage these issues.Two transistors stack configuration for the NMOS devices is illustrated in Figure 5.

In Figure 5, V_X is the intermediate node voltage.The value of $V_X$is small positive due to small drain current. Small amount of V_X voltage changes the effective terminal voltages of the devices. It causes to increase the threshold voltage and hence, minimising the off-state current. The off-state current is the function of the different terminal voltages of the device. The different input combinations produce the different amount of the leakage current. So, it is needed to estimate the leakage for all the input combinations to find out the total off-state current. If the number of inputs are less, then it is not a problem at all, but it is a problem for the large number of inputs. For the large number of inputs, heuristic algorithms are applied to see the least leakage input vector (Gao and Hayes 2006).

4.2. Multiple-Threshold

In a logic circuit, low-threshold device maintains the performance while the high-threshold device cuts the large leakage current. So, multiple-threshold devices are employed in a logic circuit to keep the performance at lower leakage current. This method is commonly used to reduce the leakage current in standby mode of the circuits while keeping the performance in the active mode.In standby mode,devices are on but not in working condition. Hence, leakage power dissipation must be reduced in standby mode to avoid the wastage of the energy. This method is also called sleep transistor method because high-threshold sleep transistors are used here to put the logic circuits in sleep or standby mode (Paul, Agarwal, and Roy 2006; Belleville et al. 2013). If this method is applied for the CMOS logic, then it is termed as multiple-threshold CMOS (MTCMOS) method. The connections of the sleep transistors in MTCMOS method are provided in Figure 6.

Extra high-threshold or sleep devices are connected in a specific form in MTCMOS method. Sleep transistors are connected either close to power supply or close to ground terminal. A header configuration is the configuration if the sleep transistor is close to the power supply. Similarly, a footer configuration is the configuration if the sleep transistor is close to the ground terminal. Therefore, there are total three arrangements of the multiple-threshold method which are depending on the header and footer configurations. Footer only configuration is widely used because of the low area requirement (Mutoh et al. 1995). Multiple-threshold method is also termed as the power gating method to turn-off the unused logic blocks in a logic circuit(Anis, Areibi, and Elmasry 2003; Johannah, Korah, and Kalavathy 2017).

If the sleep signal (SL) is at logic low, then header transistor will be turned-on while the footer transistor will be turned-off. In case of footer only configuration, the virtual ground voltage (V_{SSV}) is appeared close to the ground terminal. Similarly, if SL is at logic high, then header transistor will be turned-off while the footer transistor will be turned-on. In case of header only configuration, the virtual power supply voltage (V_{DDV}) is appeared close to the power supply. It means actual power rails are disconnected from the logic blocks which shows the large leakage saving in the standby mode.

Ground bounce noise and the wake-up delay are the main issues in the multiple-threshold method when the logic circuit is moving from sleep to active mode or vice versa (Sharma and Pattanaik 2015). A zigzag power gating method is applied to overcome the wake-up delay issue. In zigzag power gating method, two stages are utilised for the implementation of the logic circuits.A general configuration of the zigzag power gating method is provided in Figure 7 (Min, Kawaguchi, and Sakurai 2003; Shin, Paik, and Kim 2009).

4.3. Super cut-off method

Super cut-off method avoids the multiple-threshold devices in a logic circuit. In super cut-off method, leakage current is mitigated by using the single type of the threshold voltage devices. If this method is applied for the CMOS logic then it is termed as super cut-off CMOS (SCCMOS) (Valentian and Beignfe 2008). The idea behind this method is to put

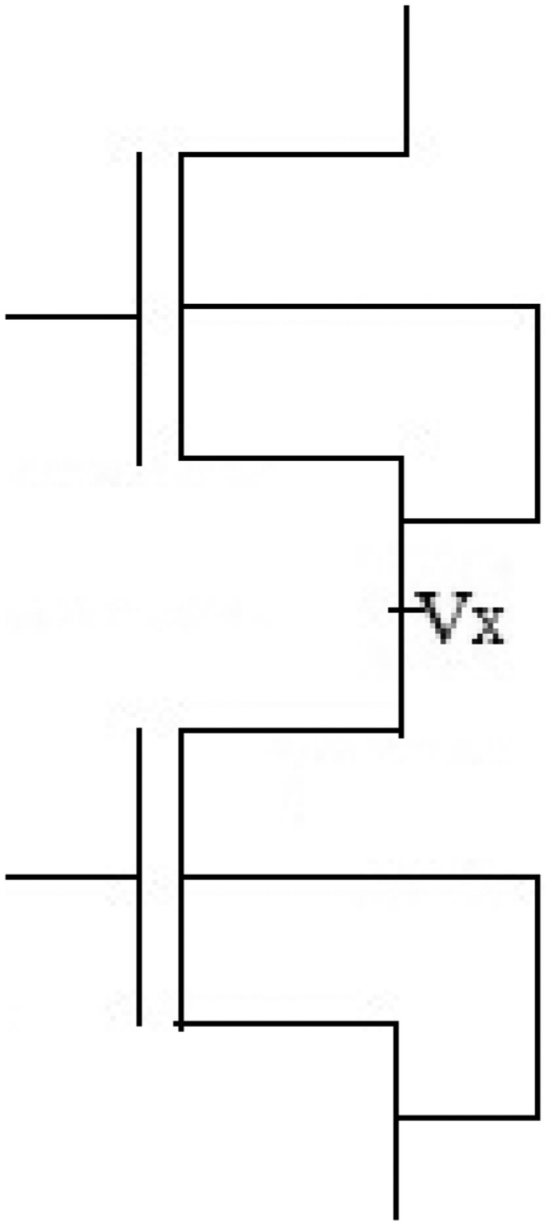

Figure 5. Two NMOS transistors stack.

the transistors in super cut-off state during the standby mode so, weak inversion current can be avoided. For that purpose, the charge pump circuit is utilised at the input of the transistors. Super cut-off state is occurred if the input voltage is less than the ground potential for the NMOS devices or the input voltage is greater than the power supply voltage for the PMOS devices (Kawaguchi, Nose, and Sakurai 2000). The charge pump circuit generates such types of the desired input signals and helps to reduce the large leakage current. The inclusion of the charge pump circuit in a logic block introduces the unwanted setup of the parameters which produces large delay (Amirabadi et al. 2004). This limits the operation of SCCMOS method specially in nanoscale regime. The logical diagram for the SCCMOS methodwhere charge pump circuit is the input of low-threshold PMOS device is shown in Figure 8.

4.4. Threshold method

Dynamic threshold method is a device-based specific configuration. It is based on the body bias concept to minimise the leakage current.In this method, threshold voltage is altered in such a way that it has the different values for the active and standby modes. The threshold voltage of the device must be high in the standby mode and low in the active mode for implementing the low power and high-performance systems. It is abbreviated as DTMOS for the CMOS logic circuits.The gate and the body terminals of the MOSFET are tightly connected in DTMOS method. The implementation of the DTMOS method depends on device level and then researchers can used it at transistor level. DTMOSisestablishedby using the triple well technology (Drake et al. 2003; Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003). An inverter is designed using DTMOS method and shown in Figure 9.

4.5. Dual-threshold method

Low-threshold device manages the performance while the high-threshold device reduces the large leakage current. Therefore, both types of the threshold voltage devices can be utilised to maintain the performance at lower leakage current. MTCMOS is such type of effort but it has the drawback of the different threshold voltage implementation in a logic circuit. Dual-threshold is very effective methodology to overcome the limitations of MTCMOS method and producing the same benefits as MTCMOS has. If dual-threshold method is used for the CMOS logic circuits then it is termed as dual-threshold CMOS (DTCMOS).The operation of the DTCMOS is based on the identification of the critical and non-critical paths in a logic circuit (Paul, Agarwal, and Roy 2006). Critical path is the path where logic is flowing, or devices are in working mode while non-critical path is the path where logic is not flowing, or path is in non-conducting mode. After the identification of the paths, high-threshold is assigned to the devices for the non-critical path while low-threshold is assigned to the devices for the critical path. The input combination can reflect the paths in a logic circuit. No additional transistor is needed in DTCMOS method for the leakage reduction (Kao and Chandrakasan 2000). Transistors stack formation in the non-critical path is responsible to reduce the large leakage current. Few algorithms are developed to get the maximum benefits of DTCMOS method(Ho and Hwang 2004). The threshold voltage assignment for the different paths is depicted in Figure 10.

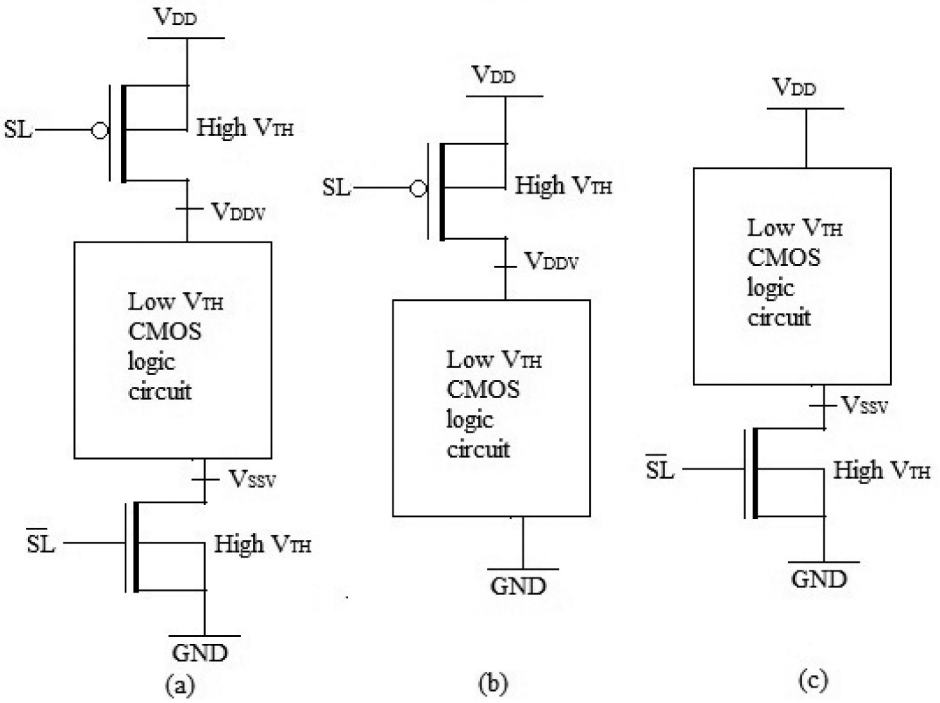

Figure 6. Multiple-threshold technique (a) with header and footer (b) header only (c) footer only.

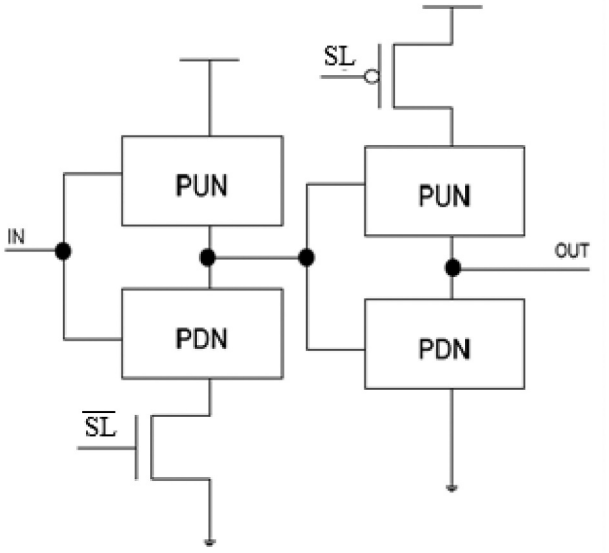

Figure 7. General schematic for the zigzag power gating method.

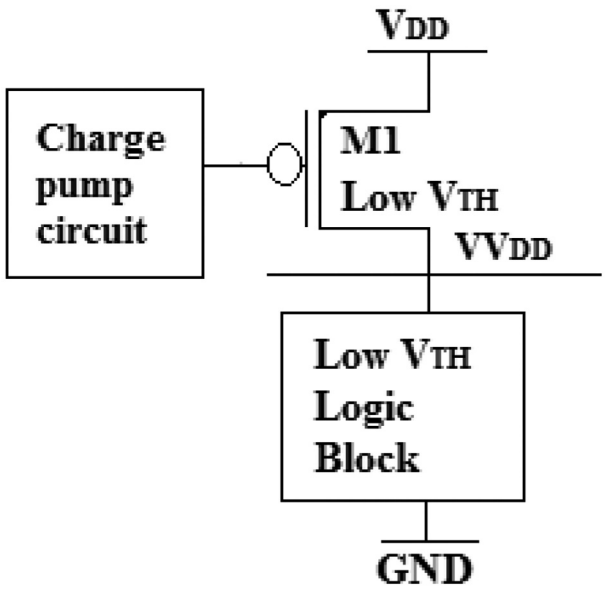

Figure 8. Logical diagram for the SCCMOS method.

4.6. Threshold method

Variable threshold method is body biased low leakage technique.In variable threshold method, body biasing is managed by the external circuit, which is connected with the body terminal of the MOSFET devices. If variable threshold method is utilised for CMOS logic, then it is termed as variable threshold CMOS (VTCMOS) method.There are the different methodologies in low power VLSI design to control the body biasing. An effective self-body bias circuit is applied in VTCMOS method. The efficiency of the VTCMOS method depends on the self-body bias circuit. Self-body bias is generated externally. External circuit implementation increases the design complexity and area. That limits its operation. The method is illustrated in Figure 11 (Im et al. 2003). The body control circuit is designed at device process level by using the triple well process.

4.7. Control point (CP) insertion method

In CP insertion, the leakage current is controlled by inserting the extra transistors to those logic gates which cause large leakage current. A logic circuit

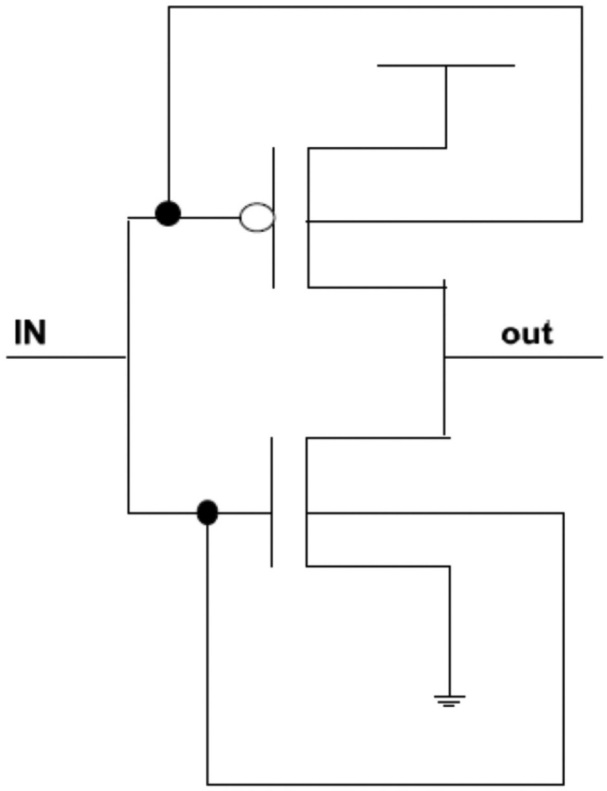

Figure 9. DTMOS inverter circuit.

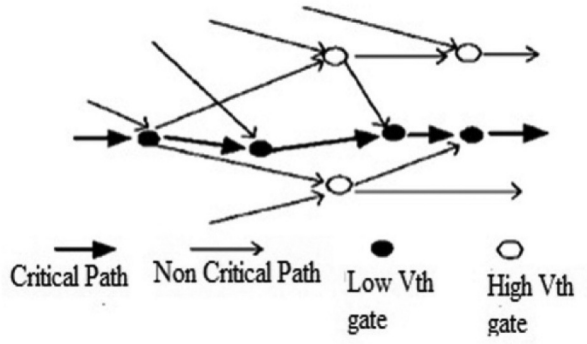

Figure 10. Threshold voltage assignment for DTCMOSmethod.

may consist number of logic gates. Few logic gates produce large leakage as compared to the others (Lin, Lin, and Li 2012).It is a difficult task to check the leakage current of the different logic gates in a logic circuit. So, some gate or transistor level approaches are employed for the calculation of the leakage current for the different logic gates. Leakage current can be minimised up to 70% if accurately select the insertion point (Rahman and Chakrabarti 2005). The insertion of CP increases the area and delay of the logic circuits.

4.8. Leakage feedback method

MTCMOS method introduces the switching issue when the operating mode is switching from standby to active mode or vice versa. The performance of the logic circuits is degraded due to high-threshold sleep

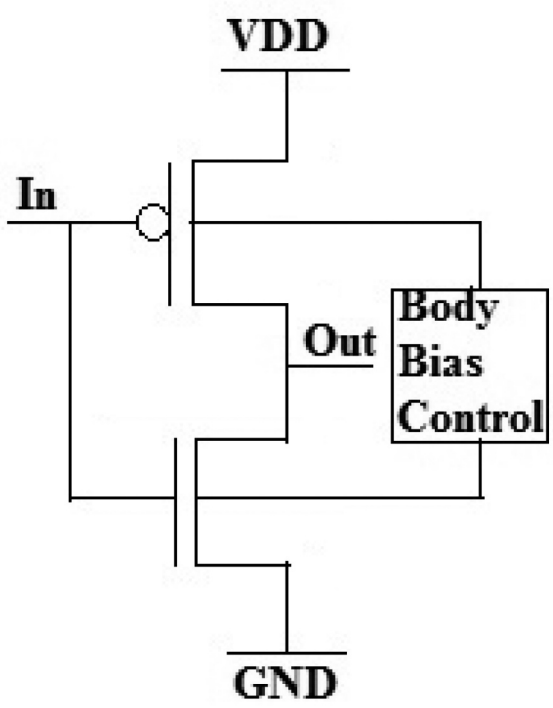

Figure 11. Self-body bias connection in VTCMOS method.

devices during the mode transitions. Leakage feedback method avoids this issue. It contains extra low-threshold devices in parallel to the high-threshold sleep devices. Low-threshold devices maintain the output characteristics during the active mode (Kao and Chandrakasan 2001). The circuit diagram of the leakage feedback method is provided in Figure 12. High-threshold sleep transistors are turned-off during the standby or sleep mode to cut the power rail/s. Extra added low-threshold device/s may be turned-on or turned-off during the modes as per the logic available at the inputs.

4.9. Sleepy stack method

Transistors stack and MTCMOS methods are the two ways to minimise the leakage current. If both the methods are applied in a logic circuit simultaneously then leakage current can be minimised by a large amount. The mixing of the transistors stack and MTCMOS method is termed as sleepy stack. In sleepy stack method, transistors are connected in a particular manner. Four high-threshold devices are additionally connected with the low-threshold circuit. Size of the high-threshold devices can be minimised to save the circuit area.Sleepy stack configuration is shown in Figure 13(Park and Mooney 2006).

High-threshold sleep transistors are connected in series with the low-threshold circuit and will be turned-off during the standby mode. During the normal operating mode, high-threshold devices will be turned-on to join the path between the power rails. An alternative configuration for the sleepy stack method is depicted in

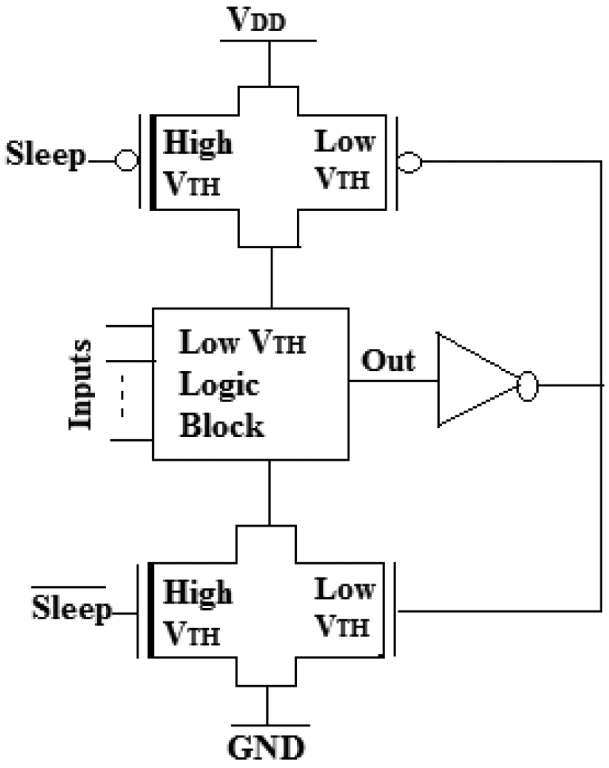

Figure 12. Transistors arrangement in leakage feedback method.

Figure 14 which shows the improvement over the sleepy stack method.This method is termed as dual sleepy stack method (Islam et al. 2010).

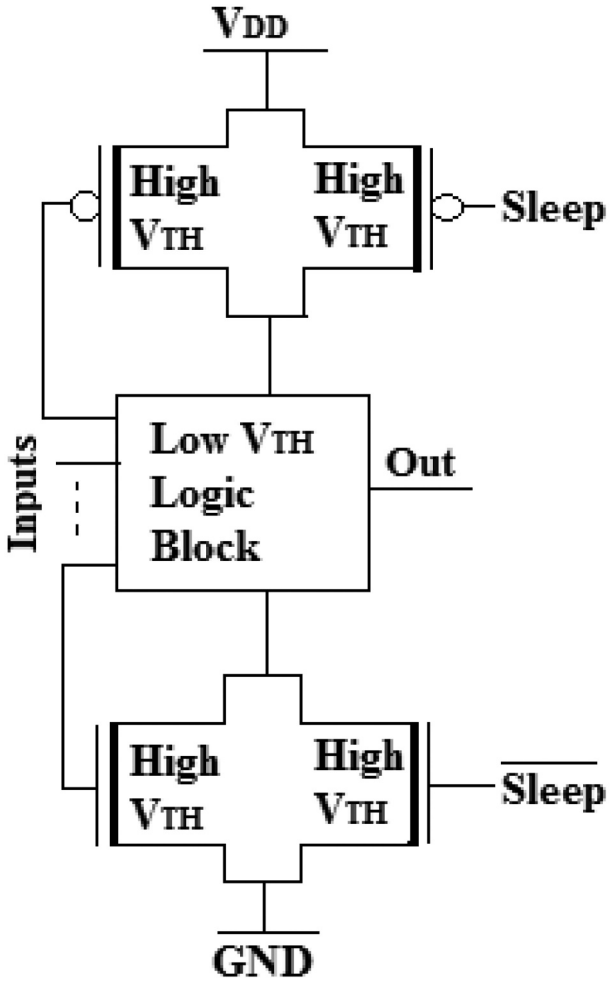

Figure 13. The configuration of sleepy stack method.

4.10. Sleepy keeper method

Four additional transistors are inserted in sleepy keeper method. High-threshold devices are connected in parallel with the low-threshold devices. The logical diagram for the sleepy keeper method is presented in Figure 15. Low-threshold devices are controlled by the output logic. Sleep transistors are in on-state during the normal mode and off-state during the sleep mode. Low-threshold devices in parallel to the high-threshold devices provide the accurate functionality (Kim and Mooney 2006). Extra inserted transistors increase the propagation delay of the logic circuits.

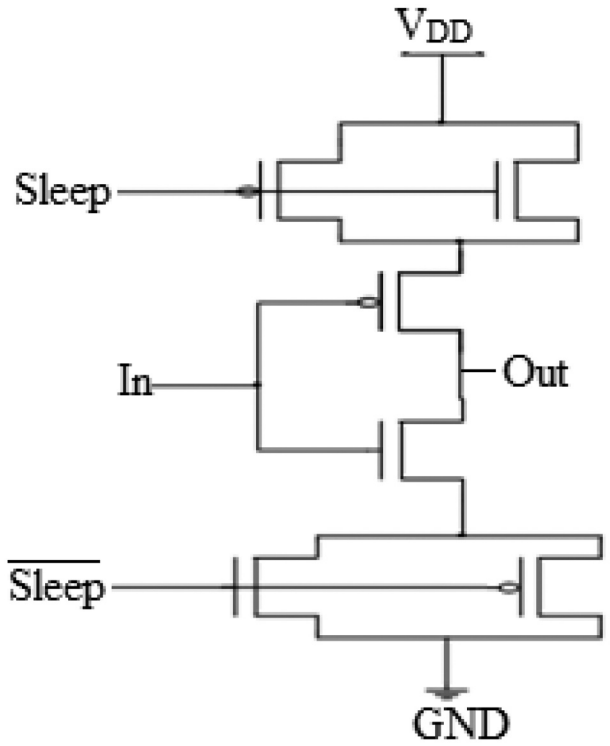

Figure 14. General structure for dual sleepy stack method.

4.11. Leakage control transistor (LECTOR) method

The basic idea behind the LECTOR method is insertion of the two additional transistors in between PUN and PDN of the CMOS logic.These extra transistors are connected in a specific arrangement in CMOS logic. LECTOR has single type threshold voltage devices throughout the logic design. Additional transistors are termed as leakage control transistors

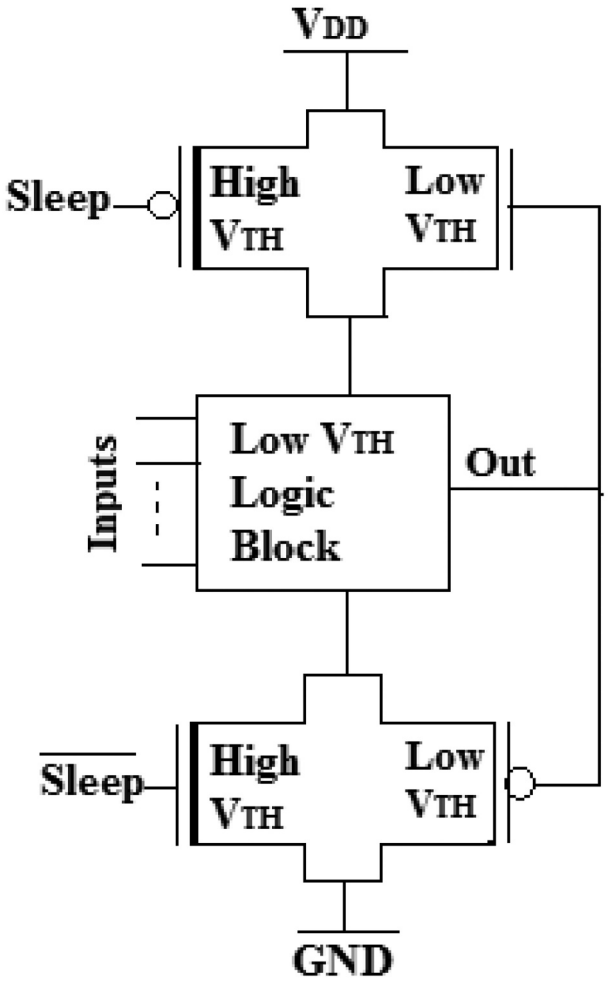

Figure 15. Logical diagram for sleepy keeper method.

(LCTs).LCTs are responsible for the leakage reduction. The logical diagram of the LECTOR method is given in Figure 16 (Hanchate and Ranganathan 2004).

The input terminals of the LCTsare joined with the source terminals of the each other. One LCT always closes to the cut-off state which helps to minimise the leakage current. The configuration of this method generates the distorted output because of the connections of the LCTs.It means noise margin is degraded in LECTOR method.

4.12. VCLEARIT method

VLSI CMOS leakage reduction technique abbreviated as VCLEARIT is the special configuration of the low-threshold and high-threshold devices for a CMOS logic. It is another way to mix the MTCMOS and stacking ideas. Three additional transistors are added in VCLEARIT method. One high-threshold PMOS device is connected in between the PUN and PDN of the CMOS logic. The logical structure of the VCLEARIT method is shown in Figure 17 (Lakshmikanthan and Nez 2007).

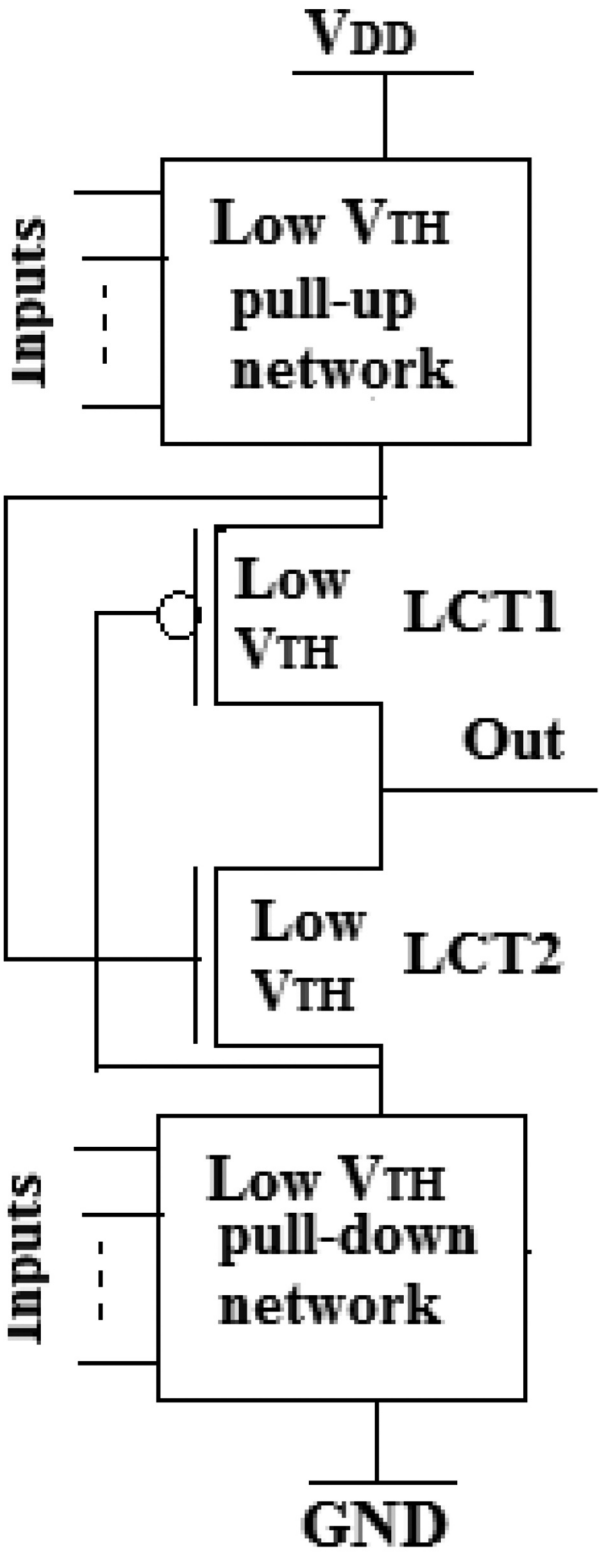

Figure 16. Logical diagram of LECTOR method.

M1 and M2 are the low-threshold transistors while M3 is high-threshold sleep transistor.M1 is connected in parallel to the PDN while M2 is connected in parallel to the PUN. These are improving the functionality of the logic circuits. M3 transistor reduces the leakage current during the sleep mode. M3 must be turned-on during the active mode. This method needs an automatic sleep signal generator as per the need of the operating modes.

4.13. Gated leakage transistor (GALEOR)method

Two high-threshold gated leakage transistors (GLTs) are utilised in GALEOR method. The logical diagram of GALEOR method is presented in Figure 18 (Katrue and Kudithipudi 2008). GLTs are attached in between the PUN and PDN of the CMOS logic. The gate and the drain terminals for the GLT are connected together.

GLTs are connected in such a manner that the output level is distorted in GALEOR method (Chun and Chen 2010). Transistors stack is the idea in GALEOR method to minimise the leakage current during the sleep mode.

4.14. Bootstrapping

Bootstrapping is an efficient method to control the leakage current by putting the devices in the super cut-off state. Bootstrapping process boosts the output levels and ideally, it is from – V_{DD} to $2V_{DD}$where, V_{DD} is the power supply voltage.Bootstrapped circuit can be used as the charge pump circuit for providing the desired input to the devices. A bootstrapped driver circuit is shown in Figure 19(Sharma and Pattanaik 2014). The output levels in bootstrapping are beyond the ground and power supply levels thus, coupling capacitors are needed for the process.

Body bias idea is used for the leakage current mitigation. Two bootstrap capacitors, C_1 and $C_2$are managing the charge from the internal nodes. At node n_4, boosted output levels are occurred. $2V_{DD}$ level is achieved at node n_4 with the help of the MN1, MN2, MP2 transistorswhile – V_{DD} level is obtained with the combination of the MP1 and MN3 transistors. Single threshold type devices are employed for the logic circuits. The input combination affects the charging and discharging of the bootstrap capacitors (Šovčík et al. 2018).

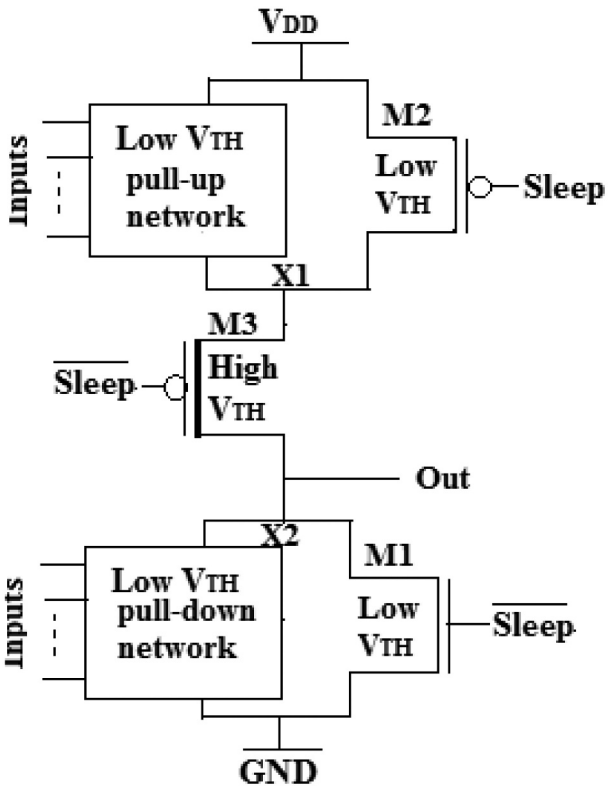

Figure 17. Logical diagram for VCLEARIT method.

4.15. On/Off logic (ONOFIC)method

The idea to mitigate the leakage current in ONOFIC method is transistors stack. Transistors stack provides the leakage reduction at the cost of delay increment. But, it overcomes the difficulty of the different threshold voltage devices implementation in a logic circuit.An ONOFIC block is additionally inserted in between the output node and PDN of the CMOS logic. ONOFIC block accurately works for the different input combinations and reduces the large leakage current. NMOS and PMOS devices are inside the ONOFIC block. Both are in on-state or off-state simultaneously. The logical diagram of ONOFIC method is depicted in Figure 20 (Sharma, Pattanaik, and Raj 2013).

The working of the ONOFIC block depends on the primary inputs available in PUN and PDN. If the output node voltage is at logic low, then ONOFIC block will be turned-on and passing the output logic to the ground potential. Similarly, if the output node voltage is at logic high, then ONOFIC block will be turned-off and avoids the discharging of the output logic to the ground potential.

4.16. Input dependent (INDEP)method

INDEP method contains two additional transistors between the PUN and PDN of the CMOS logic which are controlled by the primary inputs. Leakage current is the function of the input voltage (Mohammadian et al. 2021). Hence, each input combination has the different amount of the leakage current. If the inputs of the extra inserted transistors are managed effectively for the different primary input combinations, then large leakage can be saved. Transistors stack is the basis of this method.The logical diagram for the INDEP method is given in Figure 21(Sharma, Pattanaik, and Raj 2014; Sharma, Pattanaik, and Raj 2015). INDEP method is the single type threshold voltage technique throughout the logic circuits. The different types of the configurations in the PUN and PDN affect the inputs of the extra inserted transistors.

4.17. Input vector control (IVC) method

The basis of the IVC method is minimum leakage vector (MLV). The leakage current is the strong function of the input voltage. The different input

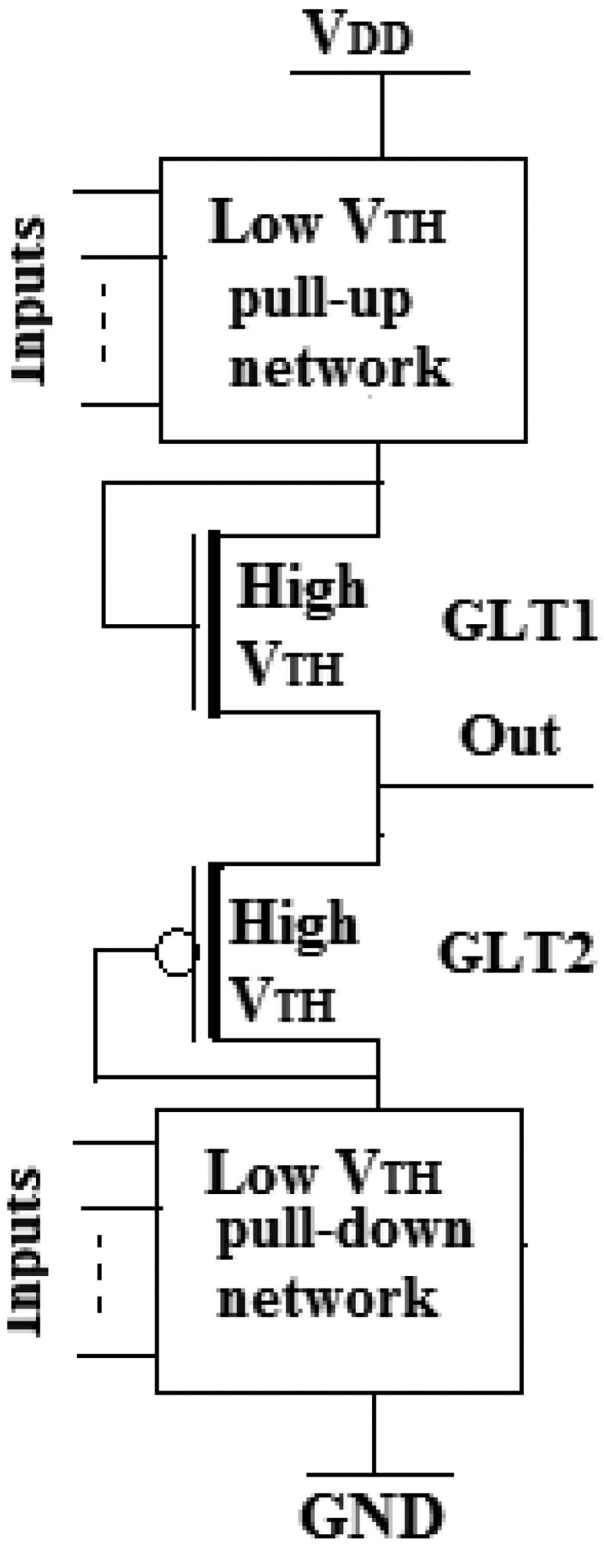

Figure 18. Logical diagram for GALEOR method.

combinations produce the different leakage current values. Therefore, MLV is calculated for the different input combinations. The logic circuit is stayed at MLV during the standby mode (Abdollahi, Fallah, and Pedram 2004; Elgharbawy and Bayoumi 2005). It causes the large leakage saving in standby mode. Transistors stack idea is utilised for the leakage saving. Off-state series connected transistors produce less off-state current (Yuan and Qu 2006). All the input combinations are checked for the leakage current for the calculation of MLV. It is possible only for the small logic circuits having few number of inputs. In case of large circuits, heuristic approaches are applied to find the MLV among the input combinations (Yang, Yu, and Peng 2016; Gulati et al. 2008). Heuristic approach iteratively checked and matched the input combinations with the last computed leakage values.

4.18. Leakage control NMOS transistor (LCNT) method

LCNT method uses two extra NMOS transistors in between the output terminal and the PDN of the CMOS logic. These transistors are connected in series form to mitigate the leakage current. The gate terminals of the extra inserted transistors are connected to the output node.Transistors stack is the basis ofLCNT method to reduce the leakage current. The logic diagram for the LCNT method is presented in Figure 22 (Lorenzo and Chaudhury 2017). Extra inserted transistors are called LCTs. LCTs will be turned-on if the output logic is high. Thus, it provides the distorted output.

4.19. Dynamic leakage-suppression logic (DLSL) method

DLSL method consists two additional transistors, one as a header and another as a footer. NMOS device is used as header while PMOS device is used as footer. The gate terminals of these extra inserted transistors are connected to the output node. If the output node is at logic low,then extra added NMOS will be turned-off and PMOS will be turned-on. Logic low at the output terminal depicts that the PDN of the CMOS is passing the logic from the output node to the source terminal of the extra added PMOS device. Similarly, extra added NMOS must be turned-on for the logic high at the output terminal so that power supply will appear at the output node. The leakage current is minimised by the super cut-off feedback mechanism(Lim et al. 2015). The logical diagram for the DLSL method is illustrated in Figure 23. The output swing voltage is degraded in DLSL method because of the locations of the extra added NMOS and PMOS transistors.

4.20. Drain gating method

In drain gating method, two extra sleep transistors are added in the CMOS logic as shown in Figure 24 (Chun and Chen 2010). During the normal operating mode, MP1 and MN1 work normally and provide the accurate output. In case of standby mode, MP1 and MN1 will be turned-off to cut-off the logic path between the power rails. Hence, leakage current reduces by a large

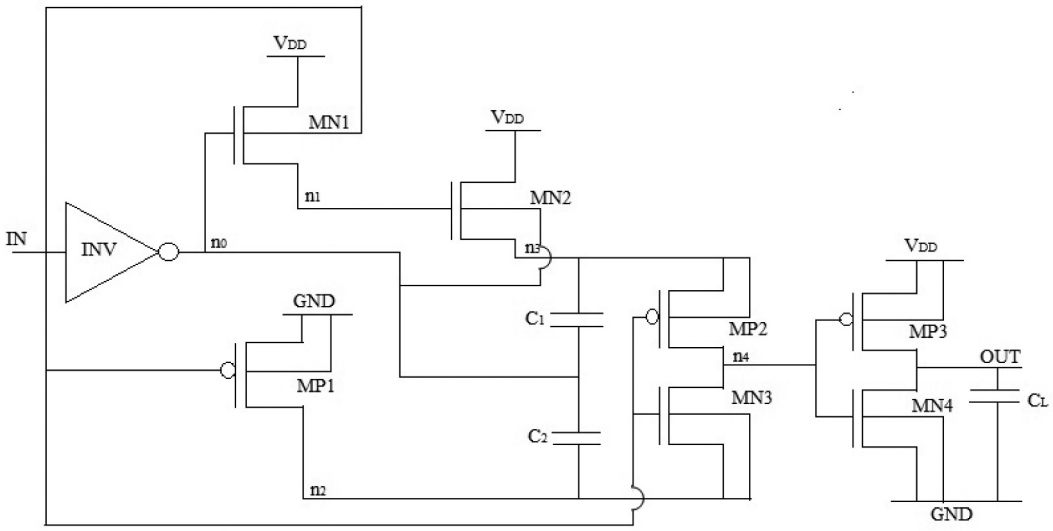

Figure 19. Logical arrangement of a bootstrapped driver circuit.

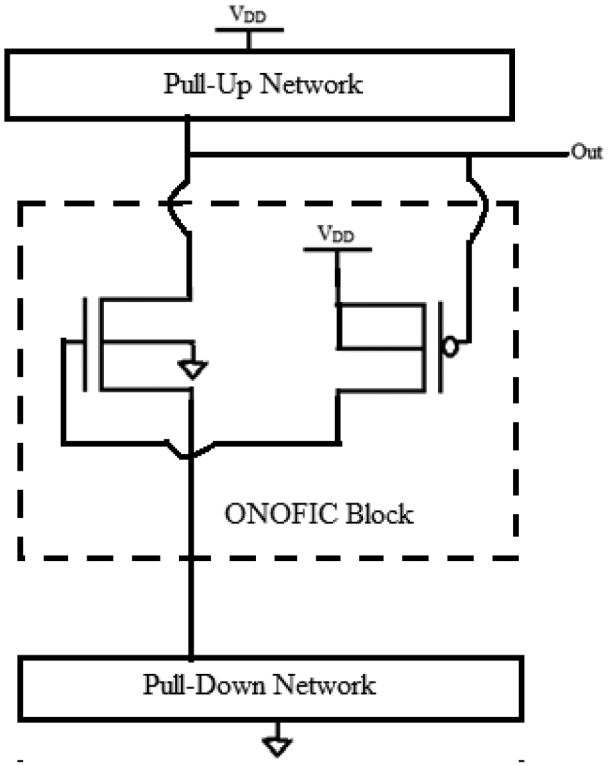

Figure 20. Logical diagram for ONOFIC method.

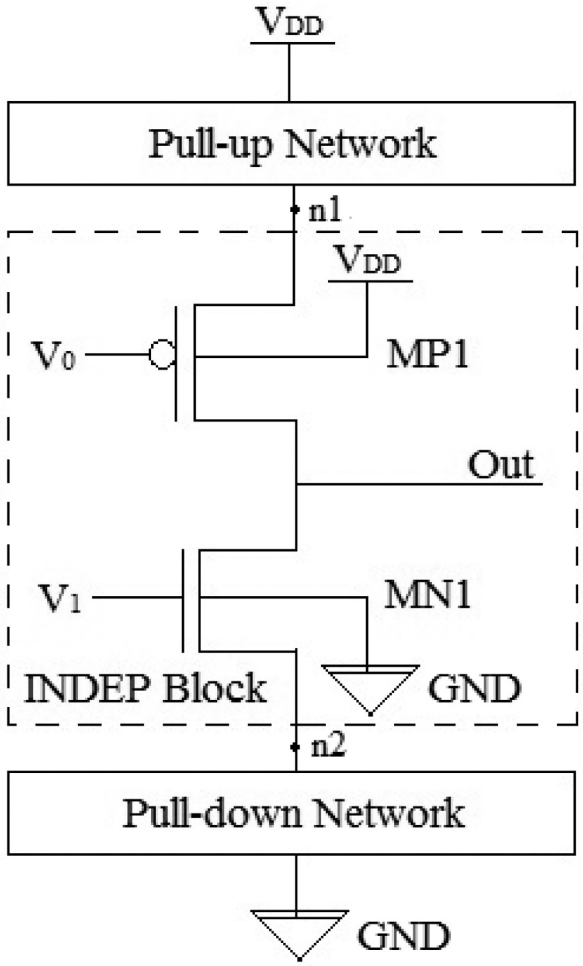

Figure 21. Logical diagram for INDEP method.

amount in standby mode.Sleep signals are inputted for the MP1 and MN1 transistors. Thus, this configuration is requiring a control block for the management of the sleep signals. That limits its operation. Transistors stack is the basic idea behind this method. This method overcomes the limitation of poor output of the LECTOR, GALEOR like methods.

5. Results and discussion

In this section,a comparative analysis is presented among the leakage reduction techniques which are discussed in section 4. A CMOSNAND3 gate is designed and simulated for the different leakage minimisation methods. A logical diagram for NAND3 gate using CMOS logic is depicted in Figure 25.

A CMOS NAND3 gate comprises three NMOS devices in PDN and three PMOS devices in PUN for the three primary inputs. In CMOS NAND3 gate,

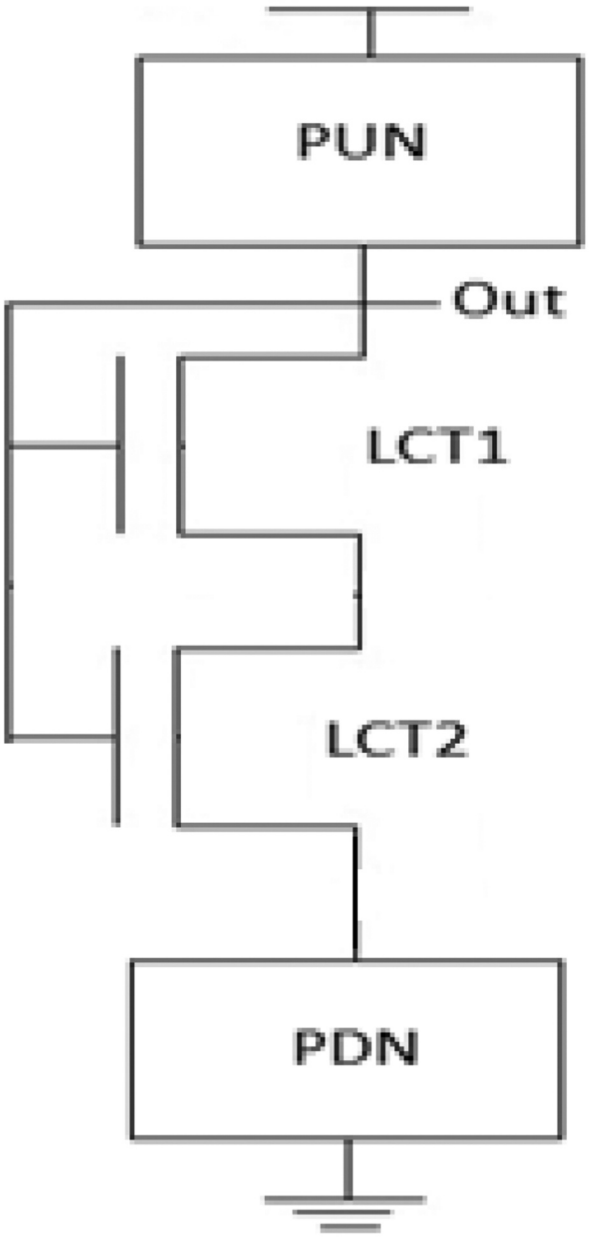

Figure 22. Logical diagram for LCNT method.

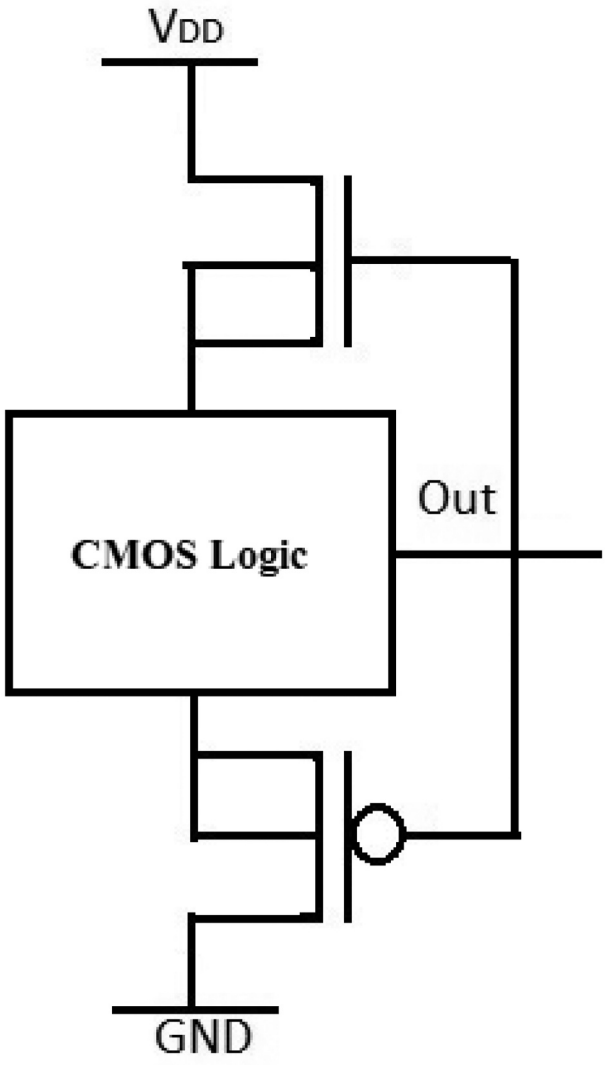

Figure 23. Logical diagram for DLSL method.

NMOS devices are connected in series while PMOS devices are connected in parallel as shown in Figure 25. NAND3 gate for the different leakage reduction techniques are designed by following the basic schematic ideas of the techniques as discussed in the section 4 as well as the logical diagram of the CMOS NAND3 gate as shown in Figure 25. The comparison among the methods is concluded for low power (LP) Berkeley Short-channel IGFET Model4 (BSIM4)Predictive Technology Model (PTM)16 nm technology node using Cadence's tools.The considered channel length for the MOSFET devices is 16 nm. The channel widths of the devices are arranged as per the channel length and these are 2× for the NMOS and 4× for the PMOS devices.The Nominal values for the power supply and the effective oxide thickness are 0.9 V and 1.2 nm respectively at 16 nm technology node. The room temperature is fixed for all the methods. For making a fair comparison among the methods, the identical parameters are assumed if needed for all the methods. The input SPICE netlists are prepared for all the methods and simulated by using Spectre circuit simulator. Leakage power dissipation (PD) and propagation delay are the key parameters specially in nanoscale regime (Kajal and Sharma 2021). Therefore, both the parameters are estimated for all the methods. The balance between them is managed by PDP. So, PDP is also calculated for all the methods. The reliability comparison is done for the PDP parameter. The simulation results for the different leakage reduction techniques are presented in Table 2.

Leakage power dissipation is calculated for all the possible input combinations. So, PD is the addition of the leakage power parts of the different input combinations. Delay is the worst value among the input combinations. PDP is the product of PD and delay values. % saving of PD and × increase in delay are estimated with respect to the conventional NAND3 gate.

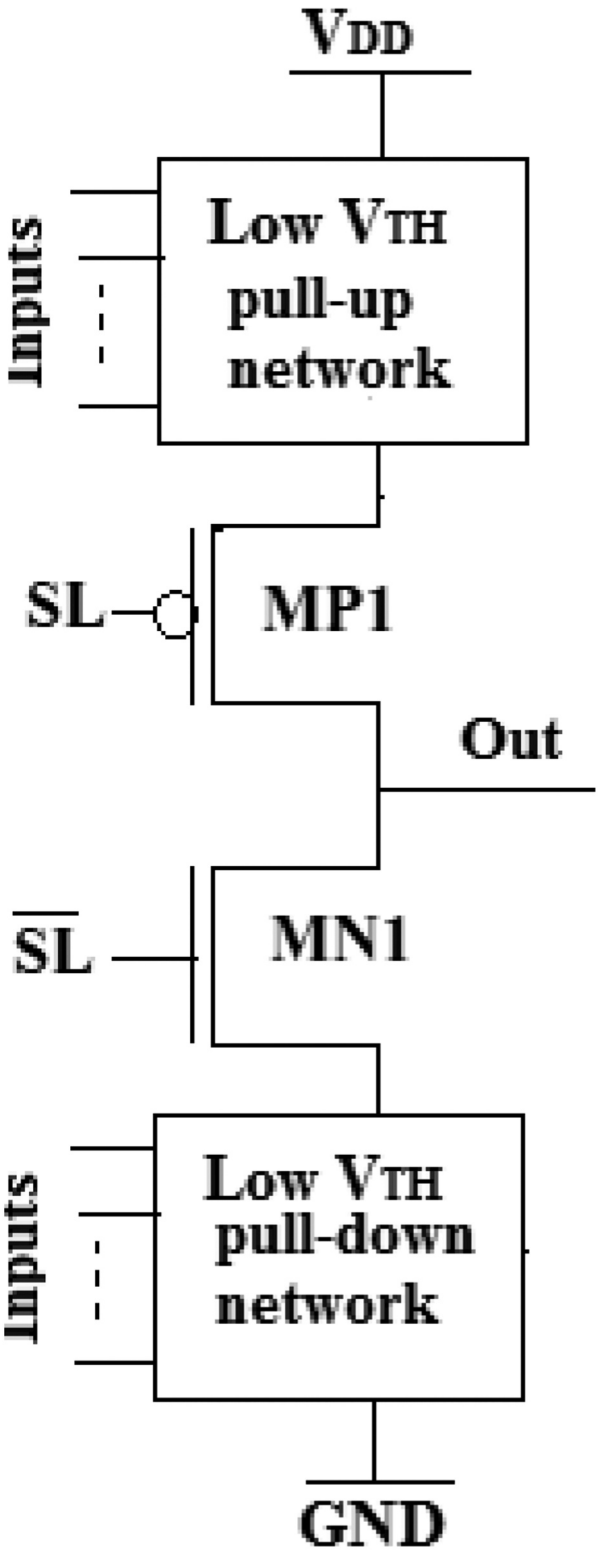

Figure 24. Logical diagram for drain gating method.

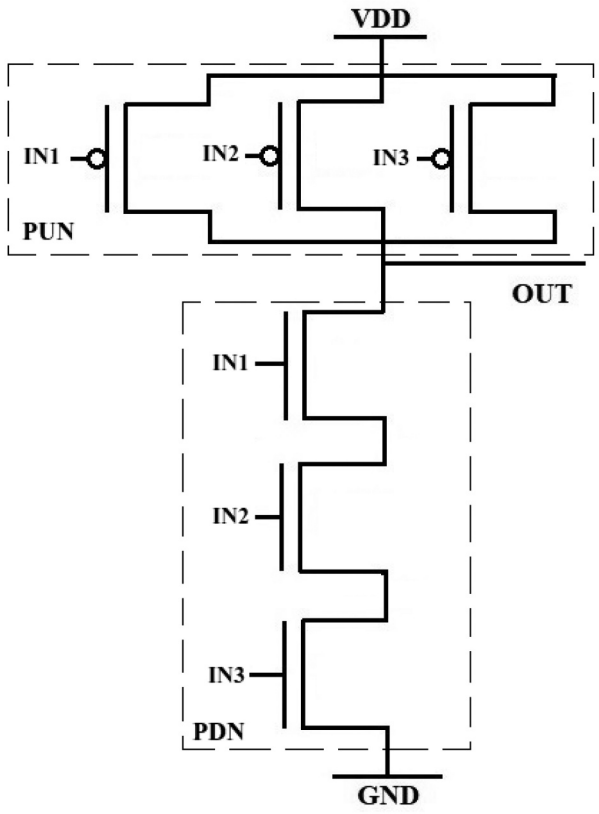

Figure 25. Logical diagram for CMOS NAND3 gate.

From Table 2, it can be observed that all the leakage minimisation methods are reducing the PD by the different amounts at the cost of delay penalty. INDEP method is showing the best PD saving followed by DTCMOS method. INDEP and DTCMOS methods are based on the critical and non-critical paths in a logic circuit. DLSL method is poor leakage saving approach followed by LECTOR method.The transistors connections in these methods are in such a way that transistors are not completely in off-state during the non-active mode.

In prospect of the delay parameter, all the leakage reduction techniques are increasing the propagation delay because of the extra insertion of the transistors and/or the time taken for the identification of the critical and non-critical paths.Ideally, delay value should be as low as possible for the high-speed operations. INDEP method has the lowest increment in the delay parameter followed by IVC method as compared to others. Sleepy stack method produces worst delay value followed by DTMOS method. High-threshold devices in sleepy stack method are increasing the delay value.Body biasing also impacts the delay value if the circuit is not stable.

PDP is the parameter which is treated as figure of merit for the logic circuits in nanoscale regime. The values of PD and delay are rapidly rising in nanoscale regime (Malik and Sharma 2020). PDP balances the trade-off between the leakage power and delay parameters. Lower value of the PDP represents the best trade-off. Table 2 shows the PDP values for the different methods.Some methods have the lower values of the PDP while others have the higher values as compared to the conventional design.It depends on the leakage saving as well as the delay value. PDP also shows the energy efficient nature of the logic circuits.The simulations results show that INDEP is the most energy efficient leakage reduction technique followed by DTCMOS. It is due to the fact that both

Table 2. Simulation results for the different leakage reduction techniques for NAND3 gate.

Method	PD (nW)	Delay (ps)	PDP (aJ)	% saving PD	× increase delay	Uncertainty
Conventional	54.06	144.01	7.79	-	-	0.81
Stacking	30.35	220.72	6.70	43.86	1.53	0.55
MTCMOS	21.21	342.23	7.26	60.77	2.38	0.68
SCCMOS	21.46	334.06	7.17	60.30	2.32	0.67
DTMOS	28.42	351.09	9.98	47.43	2.44	0.81
DTCMOS	9.89	212.36	2.10	81.71	1.47	0.45
VTCMOS	27.83	328.14	9.13	48.52	2.28	0.75
CP insertion	23.32	273.34	6.37	56.86	1.90	0.49
Leakage feedback	33.44	341.11	11.41	38.14	2.37	0.84
Sleepy stack	17.49	361.19	6.32	67.65	2.51	0.76
Sleepy keeper	27.33	338.37	9.25	49.45	2.35	0.80
LECTOR	36.18	261.24	9.45	33.07	1.81	0.64
VCLEARIT	29.14	339.43	9.89	46.10	2.36	0.77
GALEOR	30.51	278.00	8.48	43.56	1.93	0.71
Bootstrapping	24.13	245.30	5.92	55.36	1.70	0.61
ONOFIC	26.78	218.96	5.86	50.46	1.52	0.49
INDEP	5.12	174.32	0.89	90.53	1.21	0.40
IVC	12.73	198.17	2.52	76.45	1.38	0.45
LCNT	27.42	257.22	7.05	49.28	1.79	0.53
DLSL	39.86	283.64	11.31	26.27	1.97	0.71
Drain gating	25.74	302.52	7.79	52.39	2.10	0.55

PD and delay values are effectively controlled in INDEP and DTCMOS methods. Leakage feedback method has the worst value of PDP followed by DLSL method.

The different leakage reduction methods are also compared for the reliability operation for the NAND3 gate. The different variations impact the circuits seriously in nanoscale regime and tilt the characteristics(Kajal and Sharma 2021). Process, voltage and temperature (PVT) variations are considered for the reliability examination. The different parameters such as channel length, channel width, oxide thickness, threshold voltage, power supply and temperature are varied for PVT variations by ±10% from the nominal values to observe the reliability. Reliability is measured in term of statistical uncertainty of the logic circuits. Lower value of the uncertainty shows high reliability.

Statistical uncertainty is the ratio of the standard deviation to mean value (Mushtaq and Sharma 2021). Hence, Monte-Carlo simulations are completed for the 1000 samples to estimate the standard deviation and mean values for the 3σ Gaussian distribution. PDP is the figure of the merit so; uncertainty values are calculated for the PDP parameter. Table 2 represents the uncertainty values for the different leakage reduction techniques for PDP parameter. It can be easily seen from Table 2 that INDEP method is more reliable followed by DTCMOS and IVC methods. It is because of large reduction of the PD with the less penalty of the delay. Reliability of the methods are poor which has less saving of the PD and delay parameters.

6. Conclusion

The importance of the battery driven portable systems is increasing rapidly due to wide applicability in the different domains. High battery backup, high-speed and small size are the crucial performance parameters to check the effectiveness of the portable systems. The speed and the size of the systems are enhanced by the device scaling. But, device scaling introduces SCEs which cause large leakage power. Hence, trade-off occurs between the performance parameters. This review paper presents the basic ideas of different circuit level leakage reduction techniques.A comparison analysis among the techniques is also performed at 16 nm technology node by considering a CMOS NAND3 gate. Logic circuits are designed and simulated by using Cadence's tools with the help of LP BSIM4 PTM model file for the transistors. The key parameters such as leakage power dissipation, delay, PDP and uncertainty are estimated for the different methods. The comparison analysis is showing that INDEP method performs well as compared to the others in terms of all the performance parameters. Leakage power is saved by 90.53% with a 1.21× delay penalty in INDEP method as compared to the conventional NAND3 gate. INDEP method improves the PDP and the uncertainty values.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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